LAPORAN PRAKTIKUM
PENGANTAR SISTEM DIGITAL

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Tujuan:

- Memahami konsep rangkaian kombinasi.
- Mampu membangun rangkaian Half Adder dan Full Adder menggunakan Logisim.
- Mampu membangun dan mengenali rangkaian 4-Bit Adder dan 8-Bit Adder

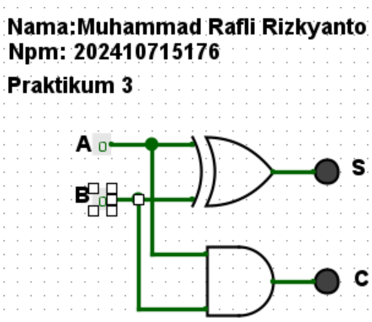
Langkah-Langkah Praktikum:

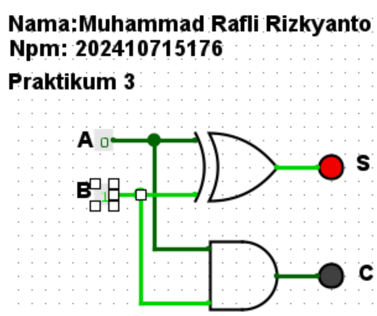
1. Mmebuat Half Adder

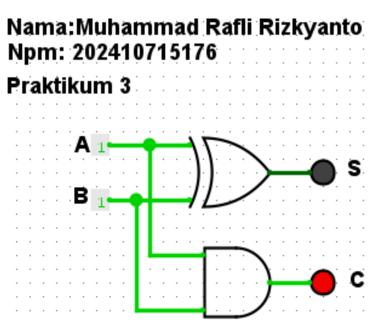
1. Rangkaian Half Adder dengan ekspresi logika
   - S=A ⨁ B (XOR)
   - C=A · B (AND)

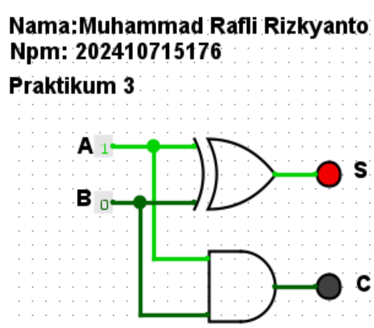
A	B	C - Carry	S - Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0
		AND	XOR

2. Gerbang Logisim-Evolution

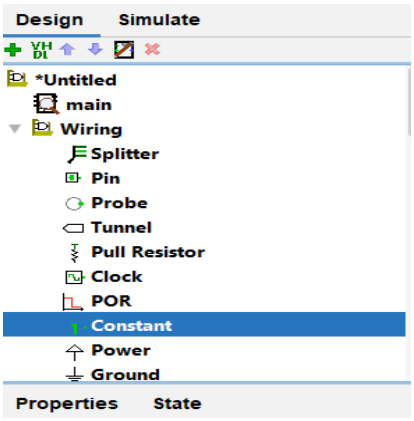




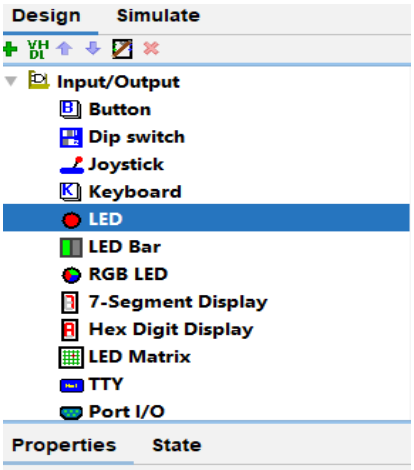




3. Hubungkan input A dan B menggunakan Constant



4. Tambahkan LED pada output S (sum) dan C (carry)

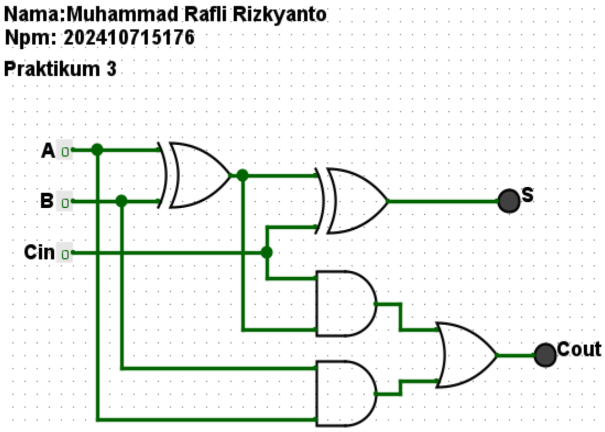


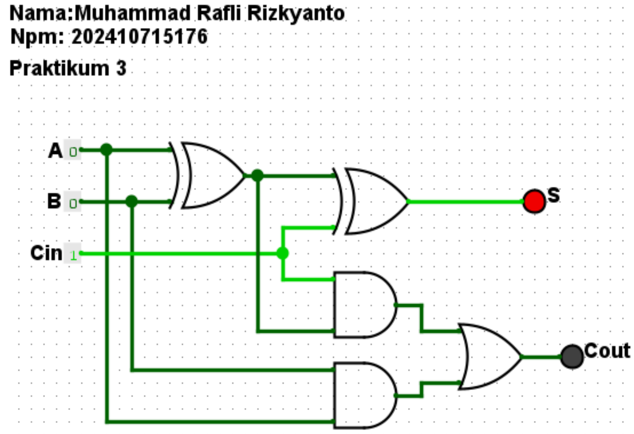
2. Mmebuat Full Adder

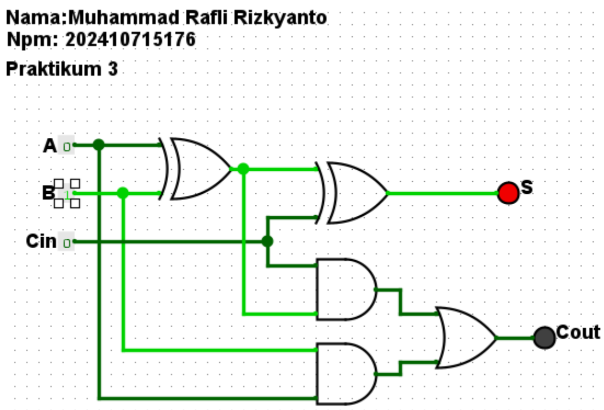
1. Rangkaian Full Adder dengan ekspresi logika
   - $S = (A \oplus B) \oplus C_{in}$
   - $C_{out} = (A \cdot B) + ((A \oplus B) \cdot C_{in})$

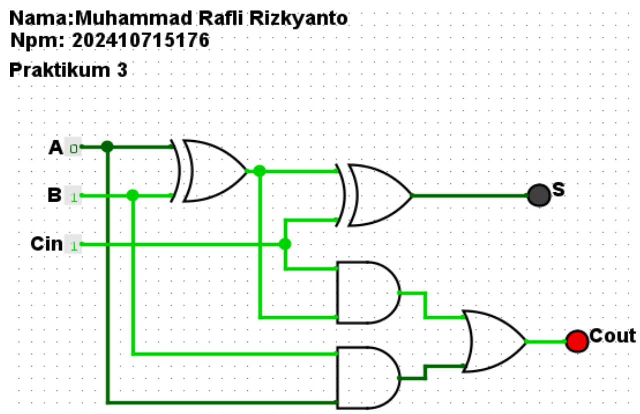
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

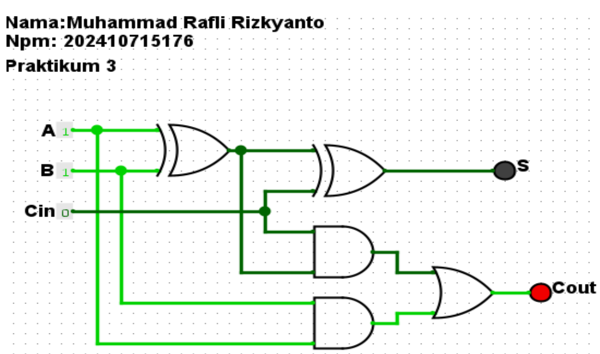
2. Gerbang Logisim-Evolution

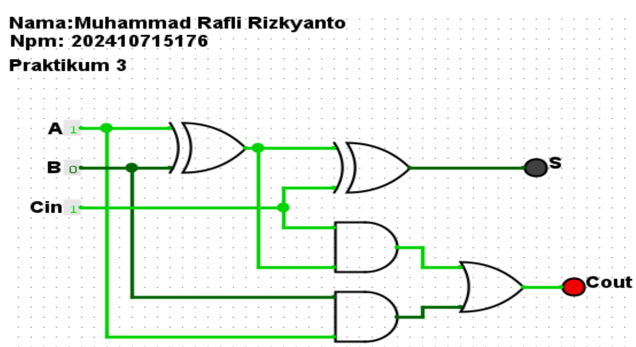


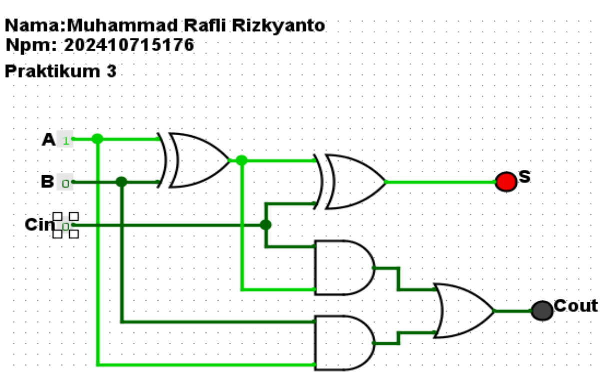


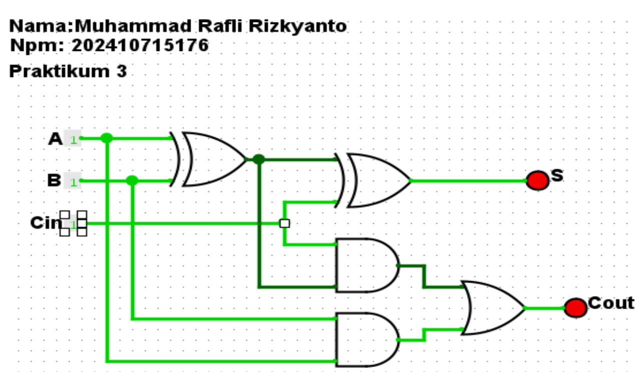




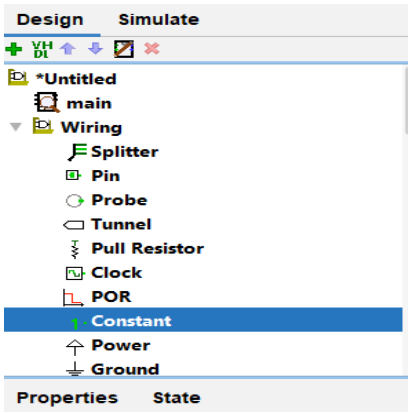




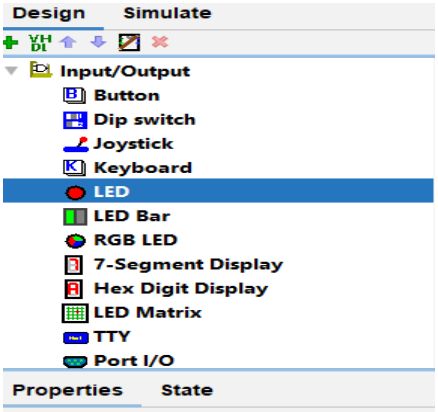




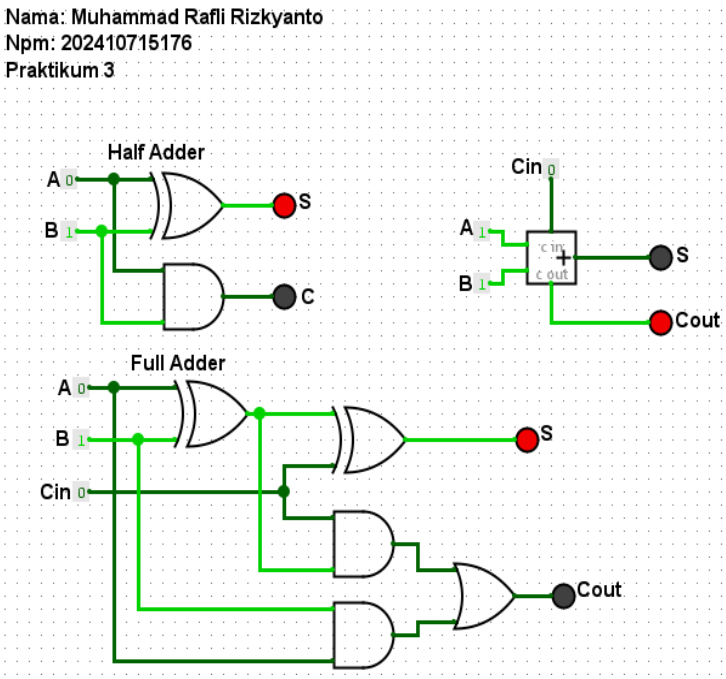
3. Hubungkan input A, B dan C_{in} menggunakan Constant



4. Tambahkan LED pada output S (sum) dan C_{out} (carry out)



5. Gambar Logisim-Evolution semuanya

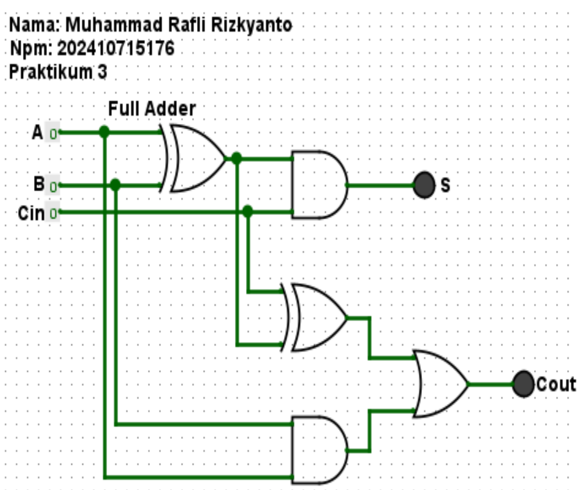


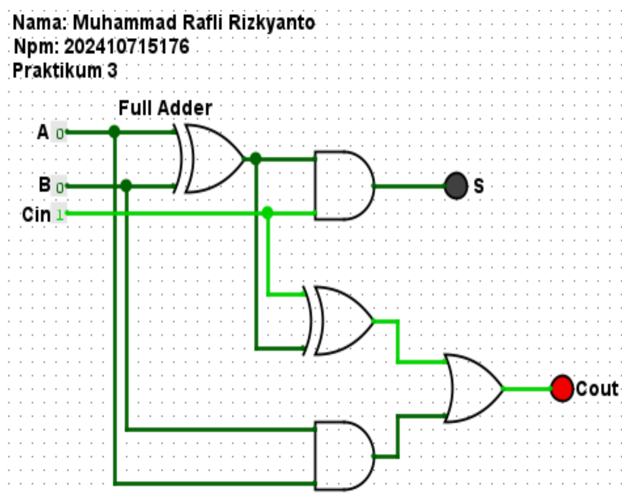
3. Rangkaian Simulasi

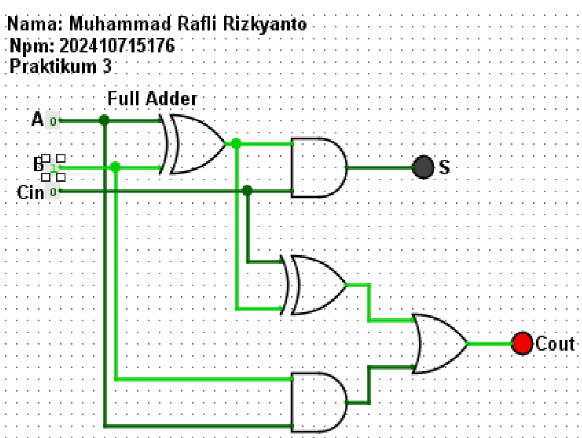
1. Rangkaian Full Adder dengan ekspresi logika
   - $S = (A \oplus B) \cdot C_{in}$
   - $C_{out} = (A \cdot B) + ((A \oplus B) \oplus C_{in})$

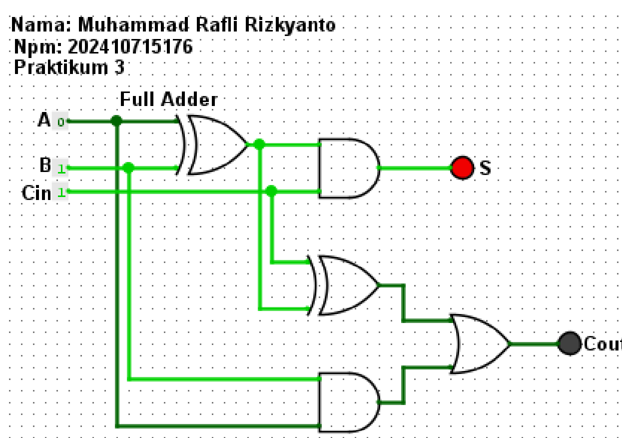
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

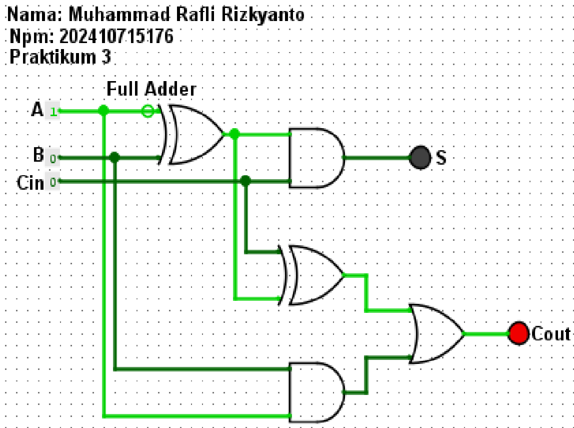
2. Gerbang Logisim-Evolution

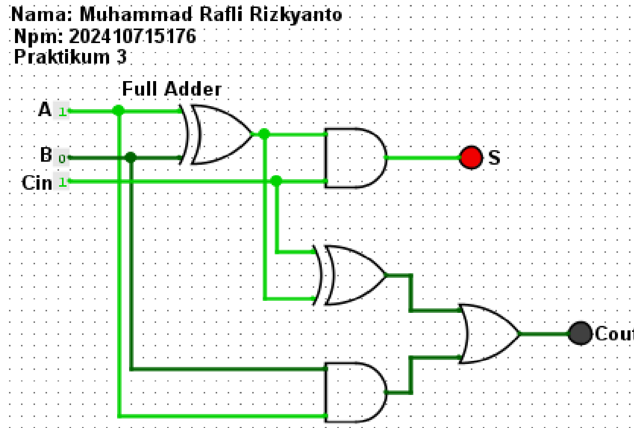


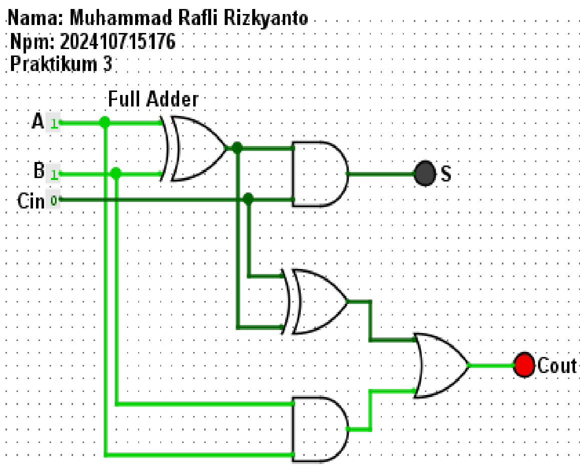


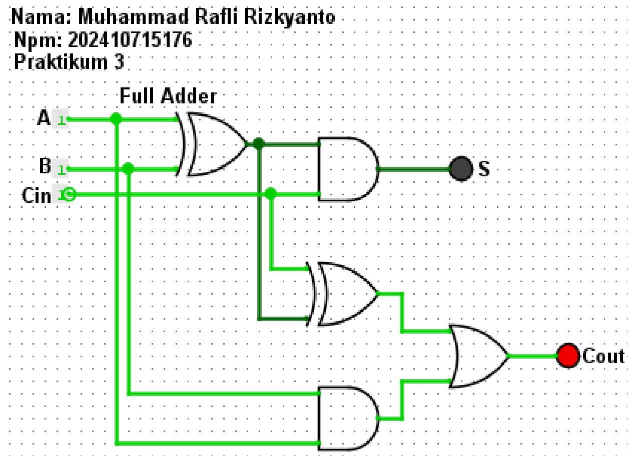




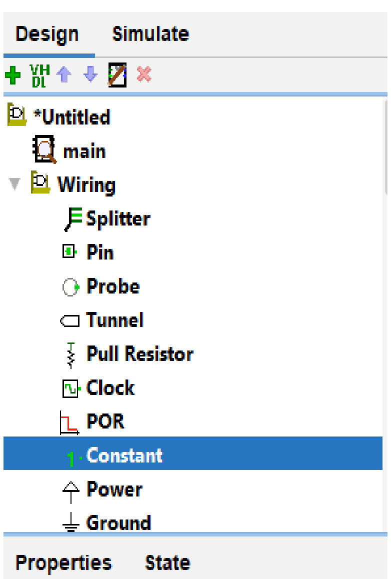




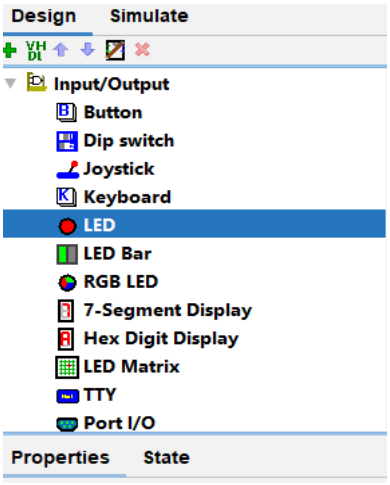




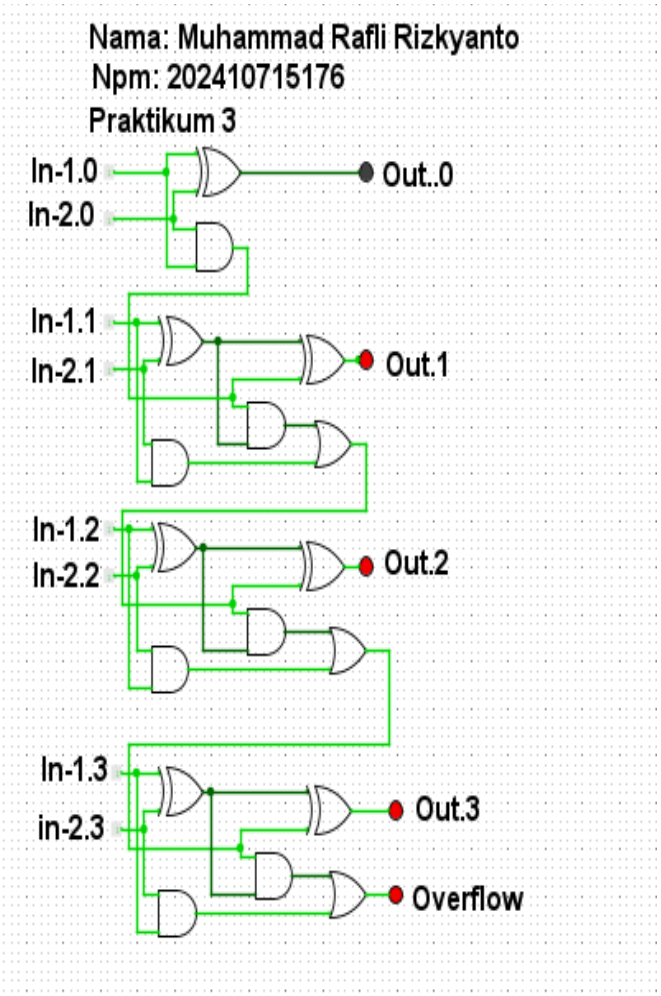
3. Hubungkan input A, B dan C_{in} menggunakan Constant



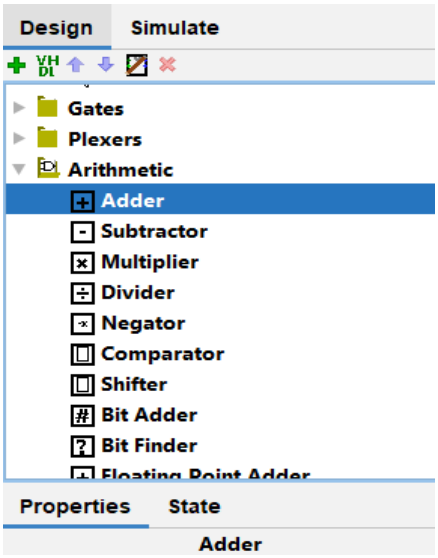
4. Tambahkan LED pada output S (sum) dan C_{out} (carry out)

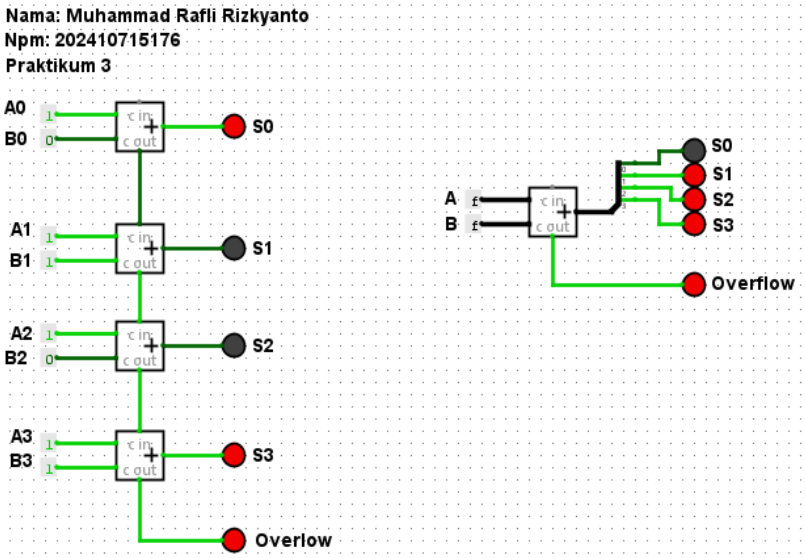


4-bit Adder



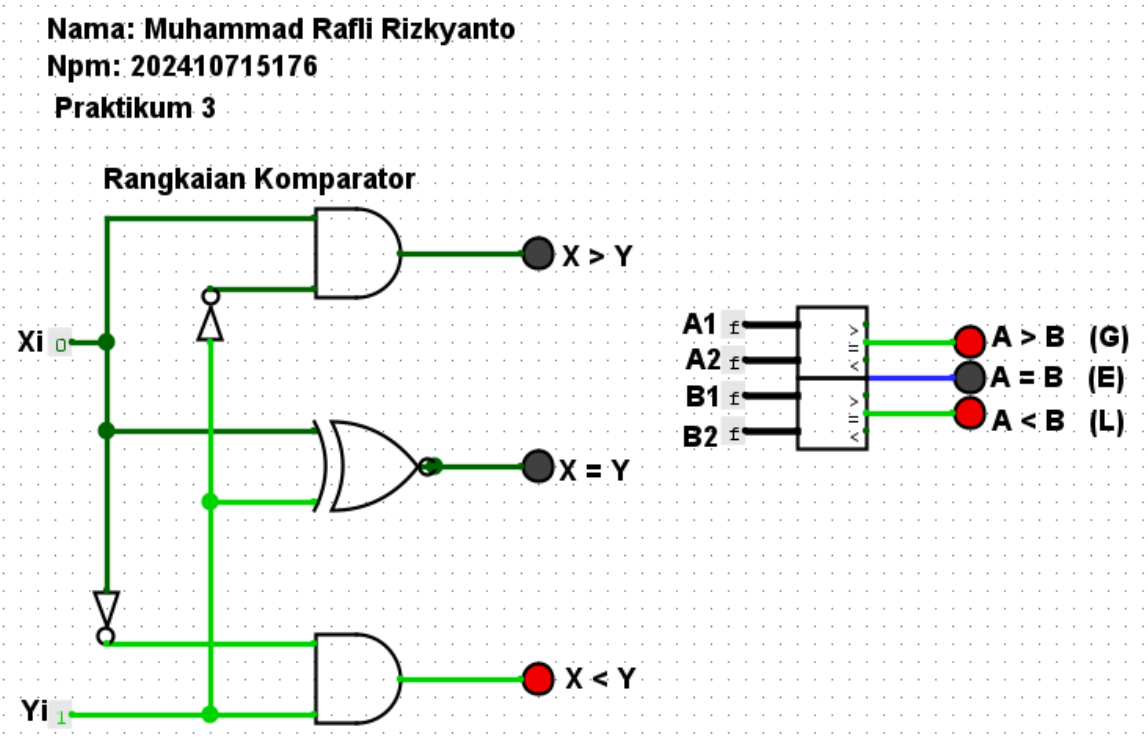
Menggunakan Komponen Aritmatika





Tabel Kebenaran Komparator

Xi	Yi	X > Y	X = Y	X < Y
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0



INPUT				OUTPUT		
(A)		(B)		(A < B)	(A = B)	(A > B)
A1	A2	B1	B2	L	E	G
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

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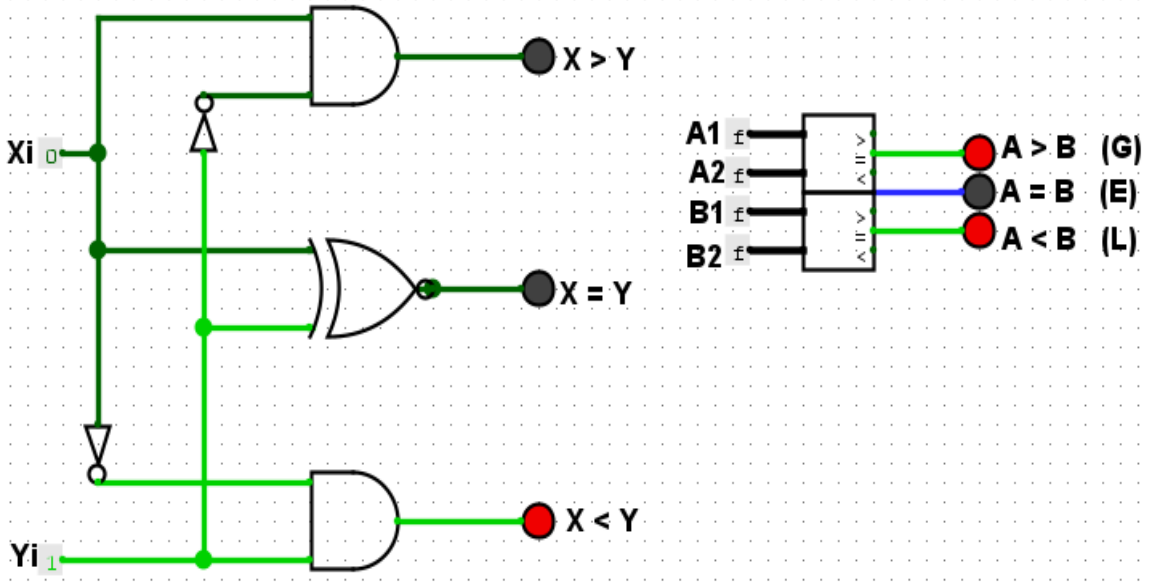
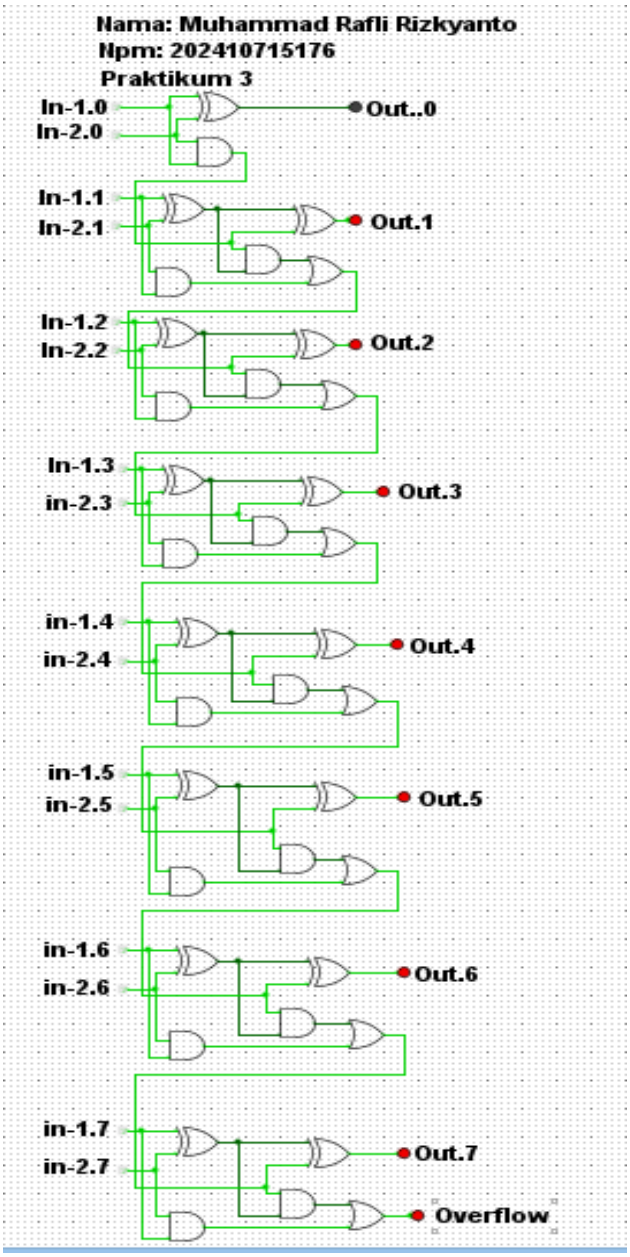
Praktikum 3

Rangkaian Komparator

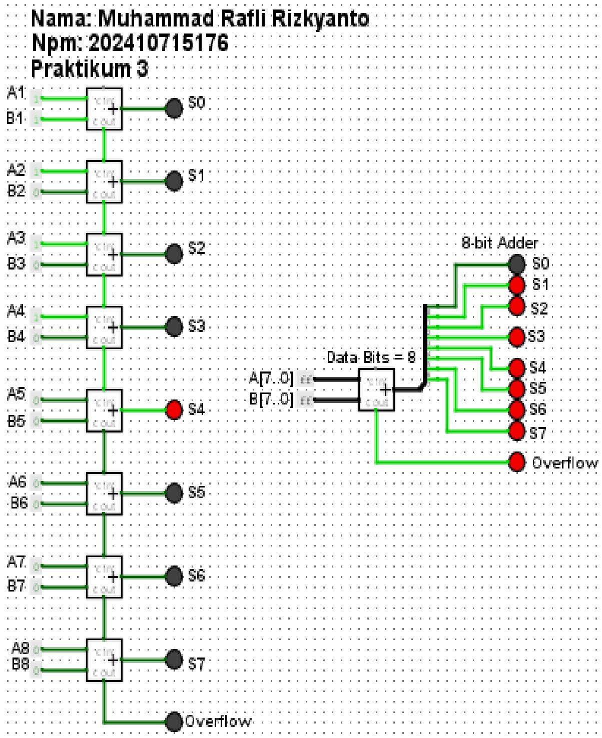


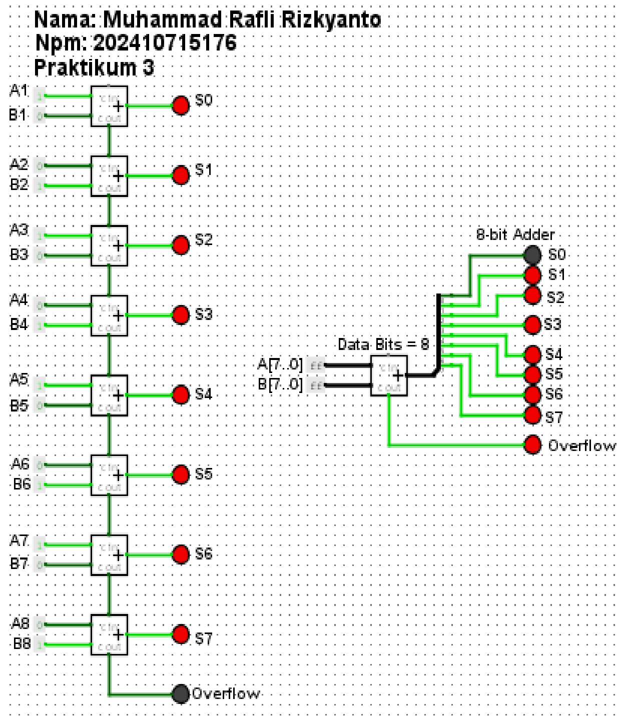
$L = -A_1B_1 + -A_1-A_2B_2 + -A_2B_1B_2$
$G = A_1-B_1 + A_1A_2-B_2 + A_2-B_1-B_2$
$E = -A_1-A_2-B_1-B_2 + -A_1A_2-B_1B_2 + A_1-A_2B_1-B_2 + A_1A_2B_1B_2$

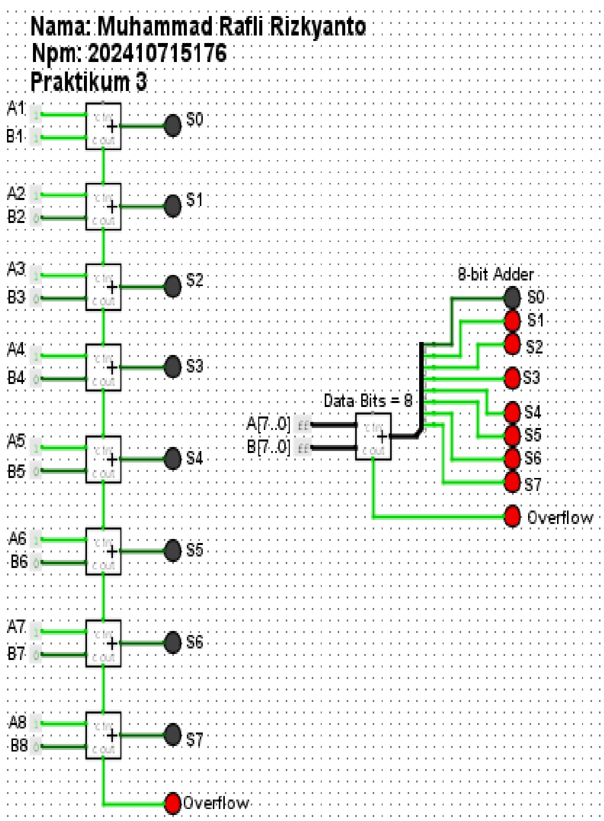
Tugas 8-bit Adder menggunakan Logisim

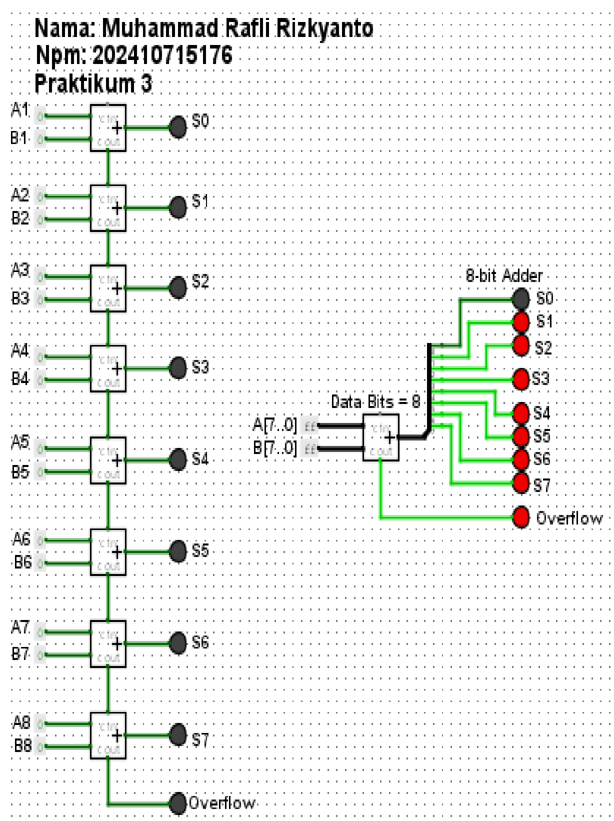


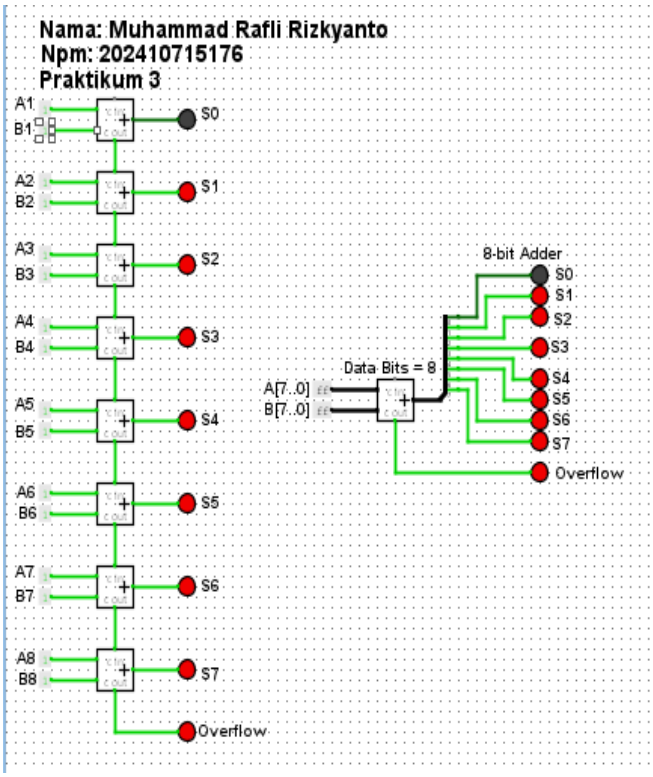
Versi Aritmatika











Tabel Kebenerannya

A (8-bit)	B (8-bit)	Cin	Hasil (S7..S0)	Cout	Keterangan
11111111	11111111	0	11111110	1	255 + 255 = 510, Overflow
11111111	00000001	0	00000000	1	255 + 1 = 256, Overflow
00001111	00000001	0	00010000	0	15 + 1 = 16, 0
10101010	01010101	0	11111111	0	170 + 85 = 255, 0
00000000	00000000	0	00000000	0	0 + 0 = 0, 0

Kesimpulan

Praktikum ini menunjukkan bahwa Half Adder, Full Adder, dan Adder multi-bit dapat dibangun dengan benar menggunakan rangkaian kombinasi di Logisim-Evolution. Semua rangkaian menghasilkan Sum dan Carry sesuai tabel kebenaran, dan pengujian 4-bit serta 8-bit Adder juga memperlihatkan proses penjumlahan biner yang benar termasuk munculnya overflow. Praktikum ini memperkuat pemahaman tentang penerapan logika kombinasi dalam rangkaian aritmatika digital.